


Form PTO-1449			ATTORNEY DOCKET NO. AUS920040060US1		SERIAL NO. 10/808,716
 LIST OF PRIOR ART CITED BY APPLICANT (Use several sheets if necessary)			APPLICANT Dimpsey et al.		
			FILING DATE March 22, 2004		GROUP ART UNIT 2182
U.S. PATENT DOCUMENTS					
EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	INVENTOR NAME	CLASS/ SUBCLASS	FILING DATE
PN	AA 5,103,394	Apr. 7, 1992	Blasciak	395/575	Dec. 21, 1989
PN	AB 6,330,662 B1	Dec. 11, 2001	Patel et al.	712/236	Feb. 23, 1999
PN	AC 6,480,938 B2	Nov. 12, 2002	Vondran, Jr.	711/125	Dec. 15, 2000
PN	AD 6,430,741 B1	Aug. 6, 2002	Mattson, Jr. et al.	717/154	Feb. 26, 1999
PN	AE 6,189,141 B1	Feb. 13, 2001	Benitez et al.	717/4	May 4, 1998
PN	AF 5,930,508	Jul. 27, 1999	Faraboschi et al.	395/706	Jun. 9, 1997
PN	AG 6,351,844 B1	Feb. 26, 2002	Bala	717/4	Nov. 5, 1998
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PN	AK 5,987,250	Nov. 16, 1999	Subrahmanyam	395/704	Aug. 21, 1997
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PN	AP 6,256,775 B1	Jul. 3, 2001	Flynn	717/4	Dec. 11, 1997
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PN	AR 6,134,676	Oct. 17, 2000	VanHuben et al.	714/39	Apr. 30, 1998
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PN	AV 5,938,778	Aug. 17, 1999	John, Jr. et al.	714/45	Nov. 10, 1997
PN	AW 6,286,132 B1	Sep. 4, 2001	Tanaka et al.	717/4	Jan. 7, 1999
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PN	BA 5,966,537	Oct. 12, 1999	Ravichandran	395/709	May 28, 1997
DATE CONSIDERED 01/26/2007			EXAMINER /Phillip Nguyen/		
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PN	BB	2002/0129309	Sep. 12, 2002		Floyd et al.	714/724 Dec. 18, 2000
PN	BC	2001/0032305	Oct. 18, 2001		Barry	712/34 Feb. 23, 2001
PN	BD	2002/0199179	Dec. 26, 2002		Lavery et al.	717/158 Jun. 21, 2001
PN	BE	2002/0124237	Sep. 5, 2002		Sprunt et al.	717/127 Dec. 29, 2000
PN	BF	2002/0147965	Oct. 10, 2002		Swaine et al.	717/124 Feb. 1, 2001
PN	BG	2002/0019976	Feb. 14, 2002		Patel et al.	717/137 May 25, 2001
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EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	COUNTRY		CLASS/ SUBCLASS	TRANSLATION YES NO
PN	BH	JP2000029731	Dec. 8, 1999		Japan	G06F 9/38 X
PN	BI	JP2000347863	Dec. 15, 2000		Japan	G06F 9/38 X
OTHER PRIOR ART (including author, title, date, pertinent page, etc.)						
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PN	BK	Cohen et al., "Hardware-Assisted Characterization of NAS Benchmarks", Cluster Computing, Vol. 4, No. 3, July 2001, pp. 189-196.				
PN	BL	Talla et al., "Evaluating Signal Processing and Multimedia Applications on SIMD, VLIW and Super Scalar Architectures", International Conference on Computer Design, Austin, Sept. 17-20, 2000, pp. 163-172.				
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PN	BN	Talla et al., "Execution Characteristics of Multimedia Applications on a Pentium II Processor", IEEE International Performance, Computing, and Communications Conference, 19 th , Phoenix, Feb. 20-22, 2000, pp. 516-524.				
PN	BO	IBM Research Disclosure Bulletin 444188, "Enable Debuggers as an Objective Performance Measurement Tool for Software Development Cost Reduction", April 2001, pp. 686-688.				
RELATED PATENT APPLICATIONS						
EXAMINER INITIAL	APPLICATION NO/ ATTY. DOCKET NO.	APPLICANT	TITLE			FILING DATE
PN	BP 09/435,069 AT9-99-491	Davidson et al.	Method and Apparatus for Instruction Sampling for Performance Monitoring and Debug			Nov. 4, 1999
PN	BQ 08/538,071 AUT919950055US1	Gover et al.	Method and System for Selecting and Distinguishing an Event Sequence using an Effective Address in a Processing System			Oct. 2, 1995
DATE CONSIDERED		01/26/2007				
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EXAMINER INITIAL	CLASS	APPLICATION NO/ ATTY. DOCKET NO.	APPLICANT	TITLE	FILING DATE
PN	BR	10/675,777 / AUS920030477US1	DeWitt, Jr. et al.	Method and Apparatus for Counting Instruction Execution and Data Accesses	Sep. 30, 2003
PN	BS	10/674,604 / AUS920030478US1	DeWitt, Jr. et al.	Method and Apparatus for Selectively Counting Instructions and Data Accesses	Sep. 30, 2003
PN	BT	10/675,831 / AUS920030479US1	DeWitt, Jr. et al.	Method and Apparatus for Generating Interrupts Upon Execution of Marked Instructions and Upon Access to Marked Memory Locations	Sep. 30, 2003
PN	BU	10/675,778 / AUS920030480US1	DeWitt, Jr. et al.	Method and Apparatus for Counting Data Accesses and Instruction Executions that Exceed a Threshold	Sep. 30, 2003
PN	BV	10/675,776 / AUS920030481US1	DeWitt, Jr. et al.	Method and Apparatus for Counting Execution of Specific Instructions and Accesses to Specific Data Locations	Sep. 30, 2003
PN	BW	10/675,751 / AUS920030482US1	DeWitt, Jr. et al.	Method and Apparatus for Debug Support for Individual Instructions and Memory Locations	Sep. 30, 2003
PN	BX	10/675,721 / AUS920030483US1	Levine et al.	Method and Apparatus to Autonomically Select Instructions for Selective Counting	Sep. 30, 2003
PN	BY	10/674,642 / AUS920030484US1	Levine et al.	Method and Apparatus to Autonomically Count Instruction Execution for Applications	Sep. 30, 2003
PN	BZ	10/674,606 / AUS920030485US1	Levine et al.	Method and Apparatus to Autonomically Take an Execution on Specified Instructions	Sep. 30, 2003
PN	CA	10/675,783 / AUS920030486US1	Levine et al.	Method and Apparatus to Autonomically Profile Applications	Sep. 30, 2003
PN	CB	10/675,872 / AUS920030487US1	DeWitt, Jr. et al.	Method and Apparatus for Counting Instruction and Memory Location Ranges	Sep. 30, 2003
PN	CC	10/757,250 / AUS920030488US1	Levine et al.	Method and Apparatus for Maintaining Performance Monitoring Structures in a Page Table for use in Monitoring Performance of a Computer Program	Jan. 14, 2004
PN	CD	10/757,192 / AUS920030543US1	DeWitt, Jr. et al.	Method and Apparatus for Providing Pre and Post Handlers for Recording Events	Jan. 14, 2004
PN	CE	10/757,192 / AUS920030548US1	DeWitt, Jr. et al.	Method and Apparatus for Determining Computer Program Flows Autonomically Using Hardware Assisted Thread Stack Tracking and Cataloged Symbolic Data	March 18, 2004
DATE CONSIDERED 01/26/2007				EXAMINER /Phillip Nguyen/	
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EXAMINER INITIAL		APPLICATION NO./ ATTY. DOCKET NO.	APPLICANT	TITLE	FILING DATE
PN	CF	10/757,227 / AUS920030555US1	DeWitt, Jr. et al.	Method and Apparatus for Autonomically Moving Cache Entries to Dedicated Storage when False Cache Line Sharing is Detected	Jan. 14, 2004
PN	CG	10/757,197 / AUS920030556US1	DeWitt, Jr. et al.	Method and Apparatus for Optimizing Code Execution Using Annotated Trace Information having Performance Indicator and Counter Information	Jan. 14, 2004
PN	CH	10/807,094 / AUS920040059US1	Dimpsey et al.	Method and Apparatus for Providing Hardware Assistance for Code Coverage	Mar. 22, 2004
PN	CI	10/806,576 / AUS920040061US1	Dimpsey et al.	Method and Apparatus for Hardware Assistance for Data Access Coverage	Mar. 22, 2004
PN	CJ	10/806,633 / AUS920040062US1	Dimpsey et al.	Method and Apparatus for Providing Hardware Assistance for Data Access Coverage on Dynamically Allocated Data	Mar. 22, 2004
PN	CK	10/806,917 / AUS920040063US1	Dimpsey et al.	Method and Apparatus for Automatic Test Case Feedback Using Hardware Assistance for Data Coverage	Mar. 22, 2004
PN	CL	10/806,871 / AUS920040064US1	Dimpsey et al.	Method and Apparatus for Hardware Assistance for Prefetching Data	Mar. 22, 2004
PN	CM	10/806,866 / AUS920040065US1	Dimpsey et al.	Method and Apparatus for Prefetching Data from a Data Structure	Mar. 22, 2004
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known

Application Number	10/808,716
Filing Date	03-22-2004
First Named Inventor	Dimpsey et al.
Examiner Name	Unknown
Art Unit	2182
Attorney Docket No.	AUS920040060US1

Examiner Initials		Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
PN	AA	5,710,881	01-20-1998	Gupta et al.	
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Examiner Initial	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

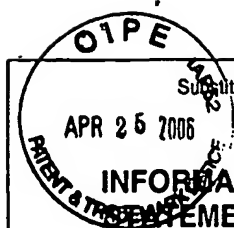
NON PATENT LITERATURE

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PN	AH	TANENBAUM, "Structured Computer Organization", 1984, Prentice-Hall, Inc., 2 nd Edition, pp. 10-12.		
PN	AI	TORRELLAS et al., "False Sharing and Spatial Locality in Multiprocessor Caches", June 1994, IEEE Transactions on Computers, Vol. 43, No. 6, pp. 651-663.		
PN	AJ	ROTHMAN et al., "Analysis of Shared Memory Misses and Reference Patterns", 2000, IEEE, pp. 187-198.		

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PN AG	Wikipedia "JavaServer Pages" downloaded 1/24/06 http://en.wikipedia.org/wiki/JavaServer_Pages
PN AH	"Hardware Cycle Based memory Residency", IBM, May 22, 2003, ip.com, IPCOM000012728D, pp. 1-2
PN AI	HYDE, "The Art of Assembly Language", 2001, Linux Edition, pp. 247-248, retrieved Mar. 1, 2005 from http://webster.cs.ucr.edu/AoA/Linux/PDFs/0_PDFIndexLinux.html

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Date Considered: 01/26/2007

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Examiner Name	Zhen, Wei Y.
Art Unit	2182
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PN AP	JEONG et al., "Cost Sensitive Cache Replacement Algorithms", June 2002, Second Workshop on Caching, Coherence and Consistency, NY, pp. 1-14.

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	Filing Date		2004-03-22	
	First Named Inventor	Dimpsey et al.		
	Art Unit	2191		
	Examiner Name	Zhen, Wei Y.		
	Attorney Docket Number	AUS920040060US1		

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
PN	1	6973417	B1	2005-12-06	Maxwell et al.			
PN	2	6721875	B1	2004-04-13	McCormick et al.			
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PN	3	6189142	B1	2001-02-13	Johnston et al.	
PN	4	5768500		1998-06-16	Agrawal et al.	
PN	5	6026235		2000-02-15	Shaughnessy	
PN	6	5950003		1999-09-07	Kaneshiro et al.	
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PN	1	20020073406	A1	2002-06-13	Gove	
PN	2	20030066055	A1	2003-04-03	Spivey	
PN	3	20030131343	A1	2002-07-10	French et al.	
PN	4	20040268316	A1	2004-12-30	Fisher et al.	

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Examiner Signature	/Phillip Nguyen/	Date Considered	01/26/2007
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Filing Date	2004-03-22
First Named Inventor	Dimpsey et al.
Art Unit	2191
Examiner Name	Zhen, Wei Y.
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